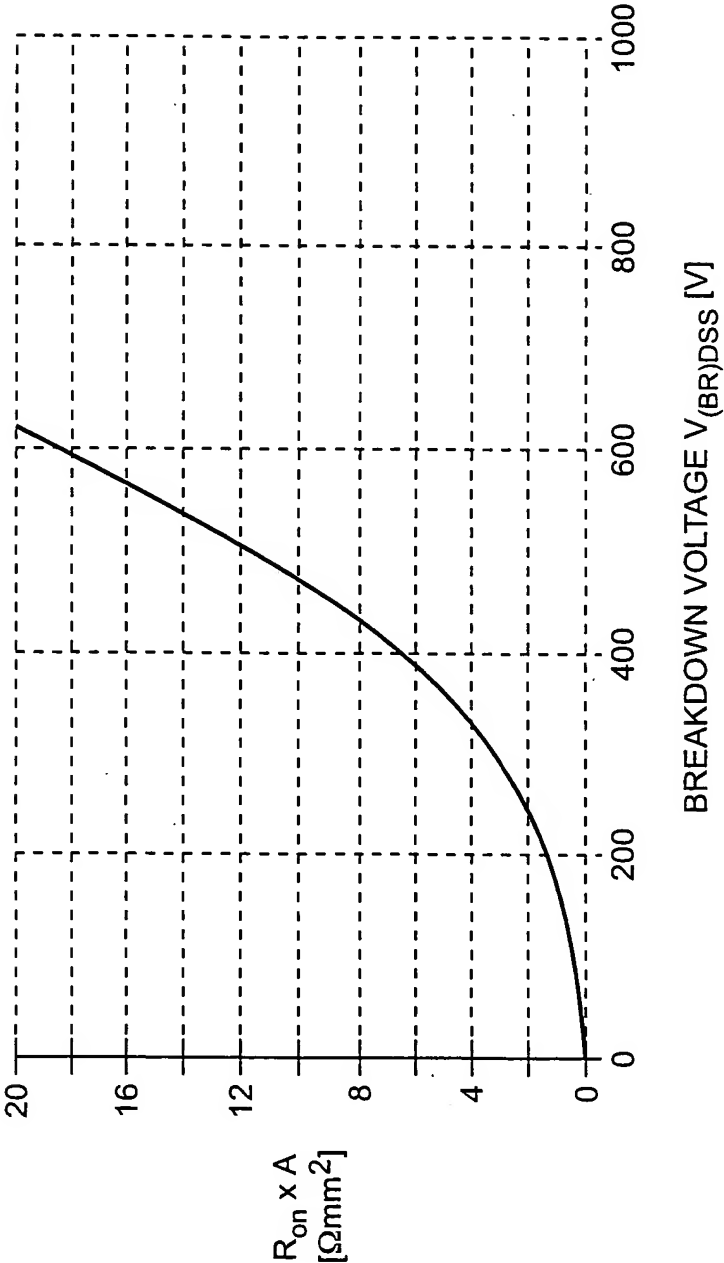


CONVENTIONAL MOSFET

FIG. 1



THE SPECIFIC ON-RESISTANCE OF A VERTICAL DMOS TRANSISTOR WITH THE DOPANT DISTRIBUTION OF FIG. 1

FIG. 2

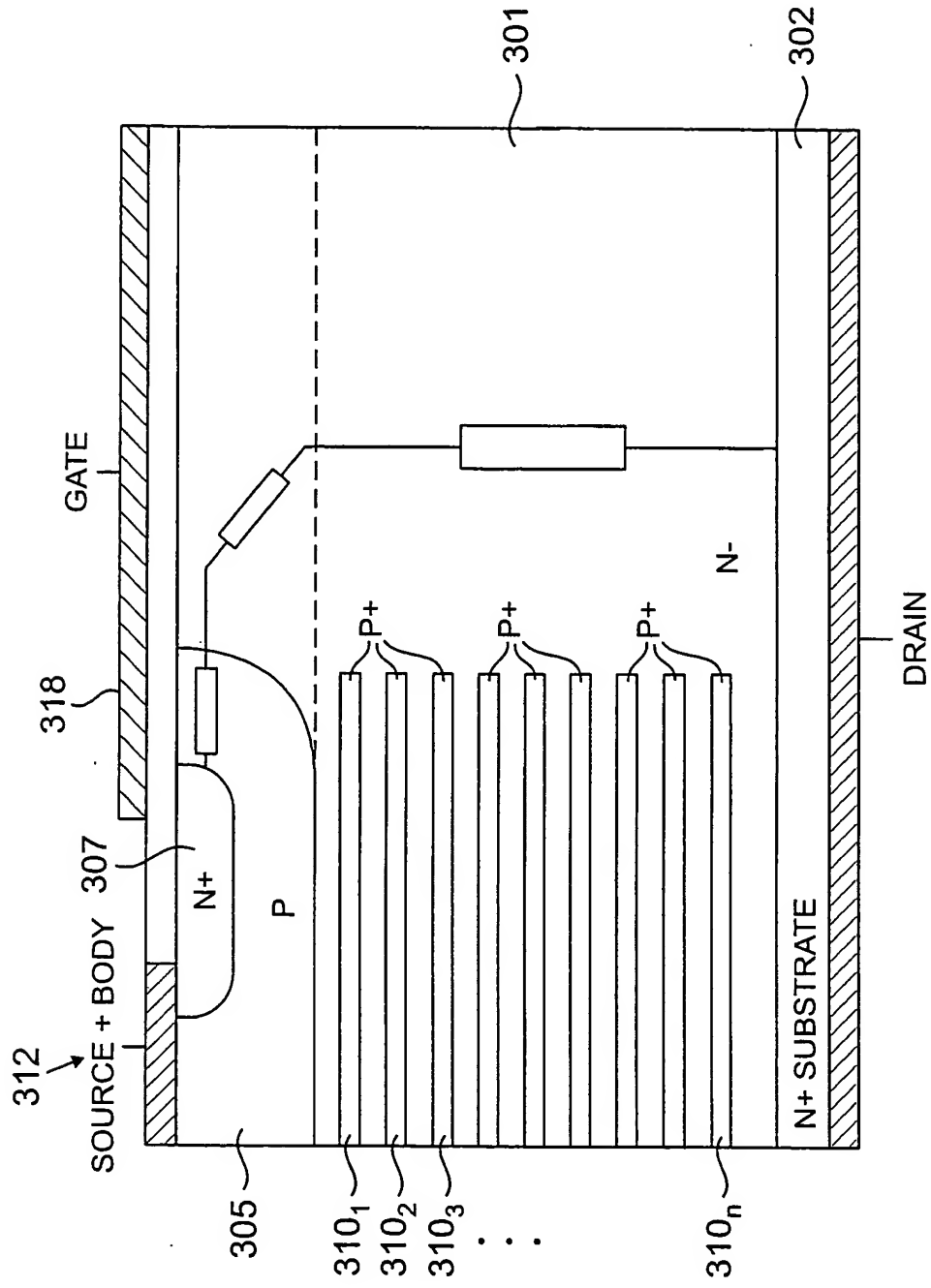


FIG. 3

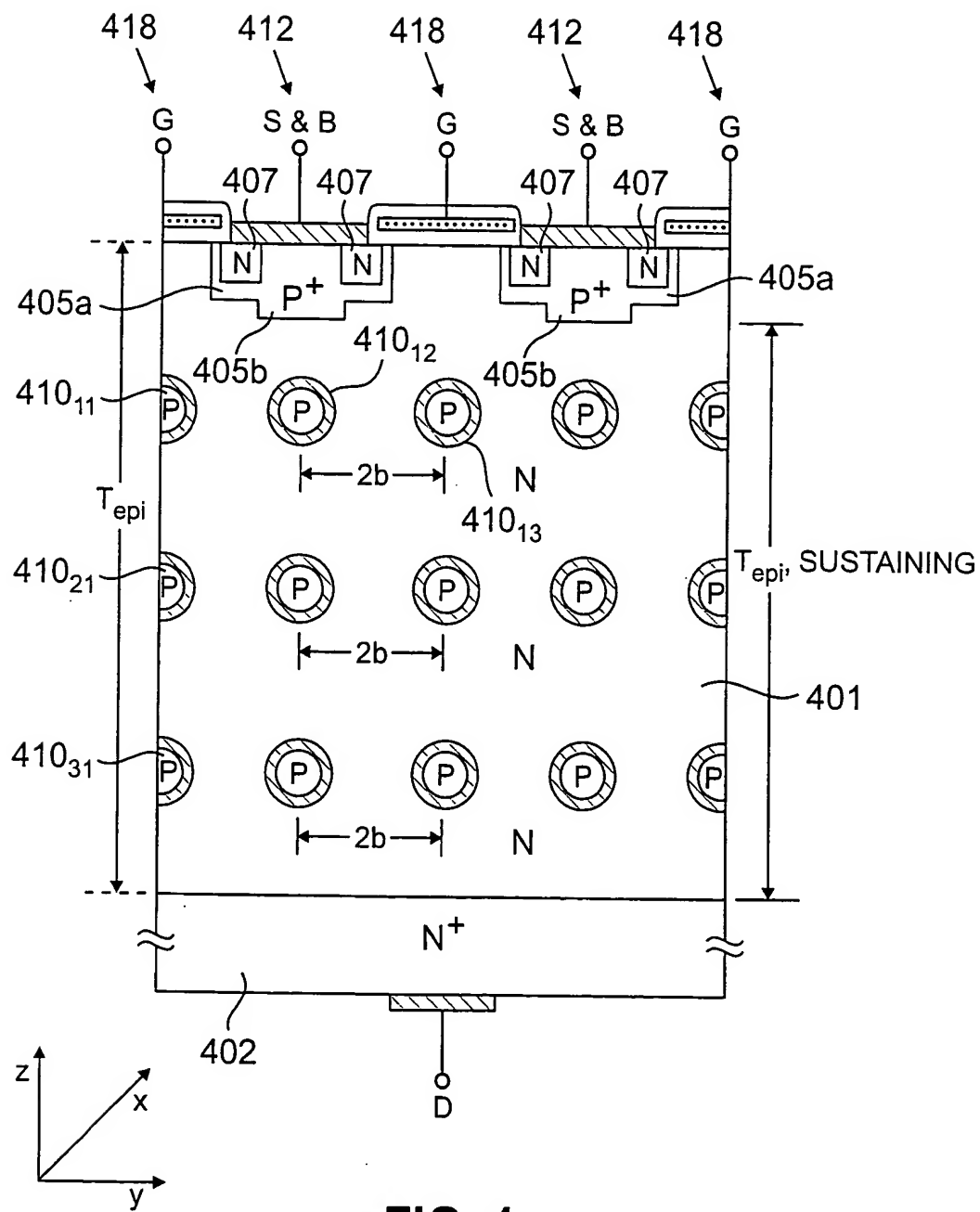
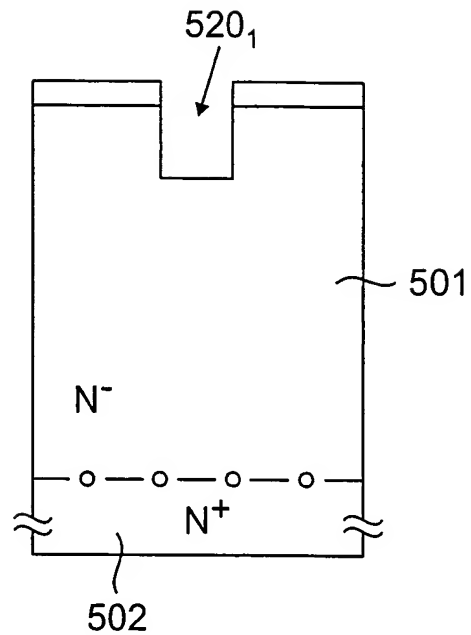


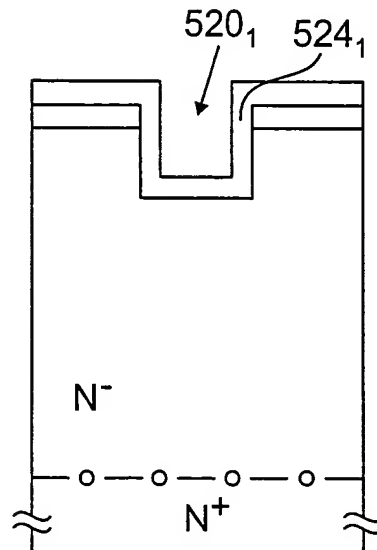
FIG. 4

STEP

1. EPITAXIAL DEPOSITION
2. FORM BARRIER LAYER
3. MASK AND ETCH THE TRENCH BARRIER LAYER
4. TRENCH ETCH

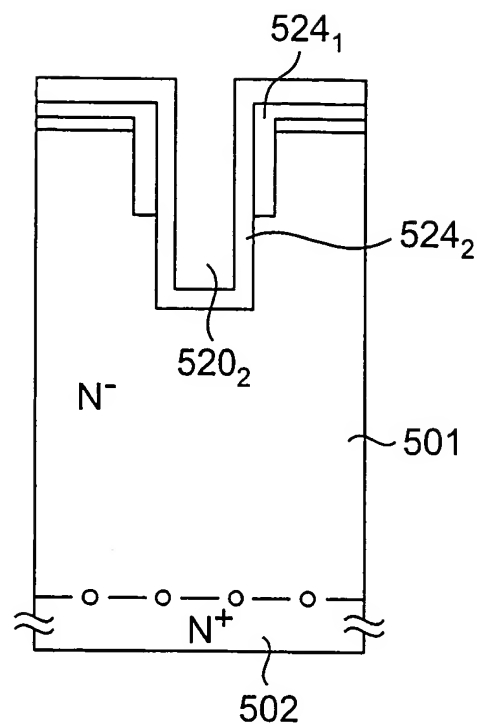
**FIG. 5(a)**STEP

5. FORM A LAYER OF MATERIAL ON THE INSIDE OF TRENCH
6. ETCH LAYER FROM TRENCH BOTTOM

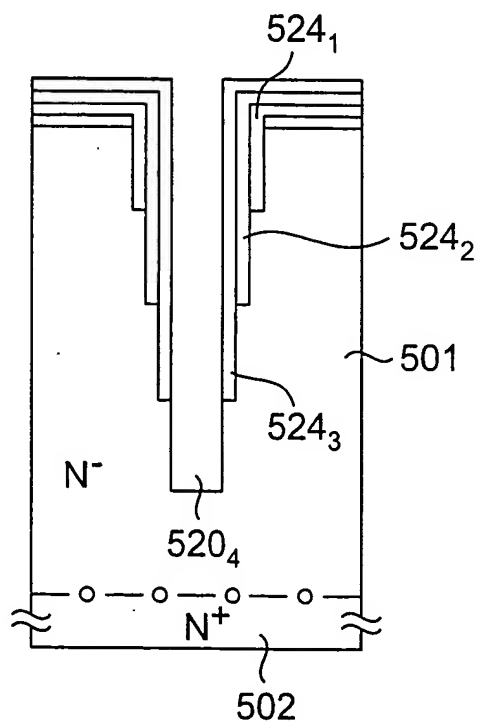
**FIG. 5(b)**

STEP

7. ETCH TRENCH
8. FORM A LAYER OF MATERIAL ON THE INSIDE OF THE TRENCH

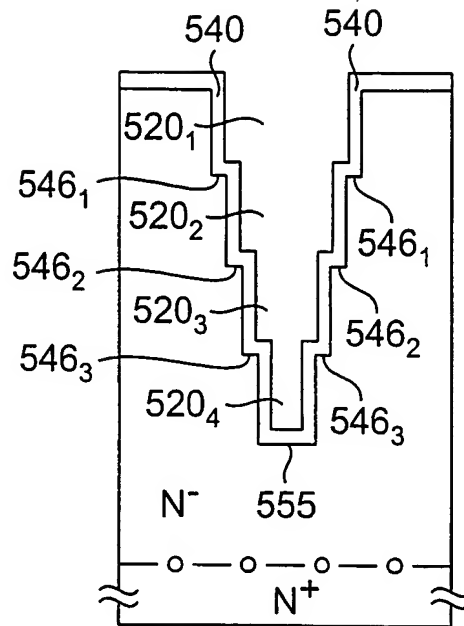
**FIG. 5(c)**STEP

9. REPEAT THE STEPS OF ETCHING THE MATERIAL FROM THE BOTTOM OF THE TRENCH, ETCHING THE SILICON TO INCREASE THE DEPTH OF THE TRENCH, AND FORMING ADDITIONAL MATERIAL ON THE SIDEWALLS AND THE BOTTOM OF THE TRENCH FOR ALL BUT THE LAST LAYER OF ISLANDS

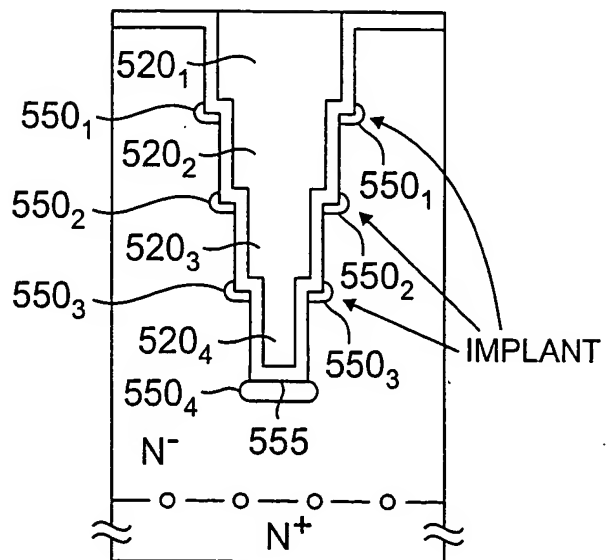
**FIG. 5(d)**

STEP

10. ETCH LAYER FROM TRENCH BOTTOM AND ETCH TRENCH
11. REMOVE ALL MATERIAL FROM TRENCH SIDEWALL
12. GROW OXIDE LAYER

**FIG. 5(e)**STEP

13. ION IMPLANTATION
14. DIFFUSION
15. FILL TRENCH
16. PLANARIZE THE WAFER

**FIG. 5(f)**

- STEP
13. ION IMPLANTATION
 14. DIFFUSION
 15. FILL TRENCH
 16. PLANARIZE THE WAFER

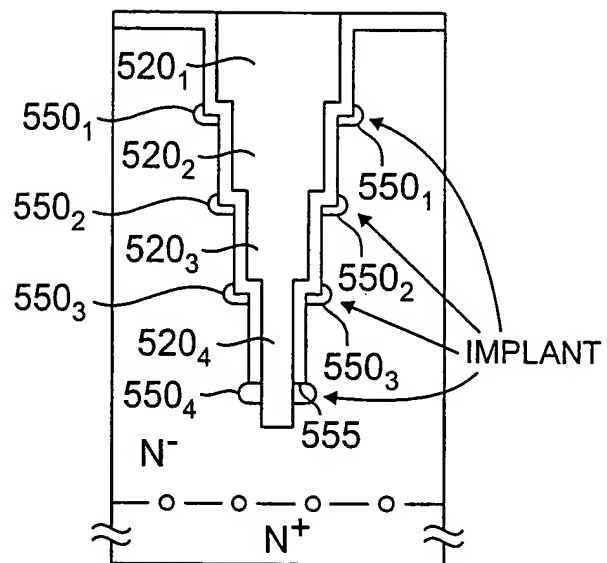


FIG. 5(g)